

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2477	checkpoint and processor	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L2	297043	high adj level	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L3	212598	low adj level	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L4	105385	(high adj level) and (low adj level)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L5	239	((high adj level) and (low adj level)) and (checkpoint and processor)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L6	52	instruction adj accurate	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L7	334	cycle adj accurate	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L8	209	((instruction adj accurate) (cycle adj accurate)) and simulat\$	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L9	0	((((instruction adj accurate) (cycle adj accurate)) and simulat\$) and (processor controller microprocessor)) and checkpoint	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L10	12431	parallel\$ same simulat\$	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L11	1050	checkpoint and partition\$	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L12	1662	((high adj level) or (low adj level)) with simulat\$4	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L13	159	rtl and (((high adj level) or (low adj level)) with simulat\$4)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L14	1251	(high adj level) with simulat\$4	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L15	545	(low adj level) with simulat\$4	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L16	134	((high adj level) with simulat\$4) and ((low adj level) with simulat\$4)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L17	218	(vhdl verilog) adj model	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L18	147	rtl adj model	US-PGPUB; USPAT	OR	ON	2005/05/12 10:44
L19	2	((("5615357") or ("6463457")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/12 10:45
L20	471	703/14.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L21	28	((high adj level) and (low adj level)) and (checkpoint and processor)) and simulator	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L22	301	703/13.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L23	307	703/22.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L24	187	((instruction adj accurate) (cycle adj accurate)) and simulat\$) and (processor controller microprocessor)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L25	45	(parallel\$ same simulat\$) and (checkpoint and partition\$)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L26	44	lauterbach and gary and sun	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L27	21	"5615357".URPN.	USPAT	OR	ON	2005/05/12 10:45
L28	5	("4500993" "5088058" "5146586" "5446876" "5448713").PN.	USPAT	OR	ON	2005/05/12 10:45
L29	91	picojava	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45

L30	101	703/19.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L31	18	((high adj level) or (low adj level)) and picojava	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L32	13	(rtl and (((high adj level) or (low adj level)) with simulat\$4)) and (((high adj level) with simulat\$4) and ((low adj level) with simulat\$4))	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L33	19	("4342093" "4527249" "4698760" "4775950" "4791593" "5047971" "5349542" "5379231" "5404310" "5535370" "5598532" "5649166" "5655109" "5696694" "5768145" "5815416" "5838947" "5949689" "6151568").PN.	USPAT	OR	ON	2005/05/12 10:45
L34	13	((high adj level) with simulat\$4) and ((low adj level) with simulat\$4) and rtl	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L35	156	703/21.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L36	63	picojava and performance and processor	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L37	19	((vhdl verilog) adj model) same processor	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L38	28	((vhdl verilog) adj model) same rtl	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L39	24	((vhdl verilog) adj model) and (rtl adj model)	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L40	13	(rtl adj model) same processor	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L41	90	717/129.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L42	37	717/135.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L43	264	717/124.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45
L44	167	717/127.ccor.	US-PGPUB; USPAT	OR	ON	2005/05/12 10:45

		Results
7.	((((pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!)) and processor) and memory) and register) and program) and content) and (branch or jump) [All Sources(- All Sciences -)]	13
6.	((((pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!)) and processor) and memory) and register) and program) and content [All Sources(- All Sciences -)]	23
5.	(((pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!)) and processor) and memory) and register) and program [All Sources(- All Sciences -)]	37
4.	(((pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!)) and processor) and memory) and register [All Sources(- All Sciences -)]	39
3.	((pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!)) and processor) and memory [All Sources(- All Sciences -)]	116
2.	(pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!)) and processor [All Sources(- All Sciences -)]	142
1.	pub-date > 1959 and pub-date < 2000 and FULL-TEXT(checkpoint) and FULL-TEXT(simulat!) [All Sources(- All Sciences -)]	422

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